What is claimed is:

1. A semiconductor memory device having full depletion type MISFETs to constitute memory cells on a semiconductor substrate via an insulating film, each of the MISFETs comprising:

a semiconductor layer formed on the insulating film;

a source region formed in the semiconductor layer;

a drain region formed apart from the source region in the semiconductor layer, the semiconductor layer between the source region and the drain region serving as a channel body in a floating state;

a main gate formed on a first side of the channel body to form a channel in the channel body; and

an auxiliary gate formed on a second side of the channel body, the second side being opposite to the first side, a portion of the second side of the channel body being capable of accumulating majority carriers under conditions in which the channel body is fully depleted by an electric field from the main gate and an electric field is applied to the channel body from the auxiliary gate,

wherein the MISFET has a first data state in which the majority carriers are accumulated in the portion of the second side of the channel body and a second data state in which the majority carriers

accumulated in the portion of the second side of the channel body are emitted,

wherein the MISFETs are arranged in the form of a matrix to constitute a cell array, the drain regions are connected to bit lines, the main gates constitute word lines intersecting the bit lines, the source regions are connected to a fixed potential line and the auxiliary gate is formed as a common electrode shared among the memory cells.

2. The semiconductor memory device according to claim 1, wherein the auxiliary gate is formed as the common electrode for the whole cell array.

3. The semiconductor memory device according to claim 1,

wherein the first data state is set by impact ionization generated near a drain junction with a pentode operation of the MISFET, and

the second data state is set by sending a forward bias current between the channel body and the drain region.

4. The semiconductor memory device according to claim 1, wherein the first side of the channel body is a top side face of the semiconductor layer, the second side of the channel body is a back

side face of the semiconductor layer and the main gate is formed on the top side face via a gate insulating film.

5. The semiconductor memory device according to claim 4, wherein the auxiliary gate is an impurity diffusion layer formed on the semiconductor substrate.

6. The semiconductor memory device according to claim 4, wherein the auxiliary gate is an impurity doping layer buried between the semiconductor substrate and the insulating film.

7. The semiconductor memory device according to claim 1, wherein each of the memory cells is a unit of storing one bit data and each of the memory cells consists of one full depletion type MISFET.

8. The semiconductor memory device according to claim 1, wherein the auxiliary gate is connected to an auxiliary gate terminal to which a constant voltage is applied.